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Potharaju

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(54) **SOLAR INVERTER**

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(52) **U.S. Cl.**

CPC **H02M 7/5395** (2013.01); **H02M 7/4807** (2013.01); **H02M 7/5387** (2013.01)

(58) **Field of Classification Search**

CPC . H02M 7/5387; H02M 3/1584; H02M 3/285; H02M 7/493; H02M 7/4807; H02M 7/49; H02M 7/5395; H02J 1/12; H02J 1/102
USPC 363/15, 39–40, 5, 71–72, 98, 132, 95, 363/131

See application file for complete search history.

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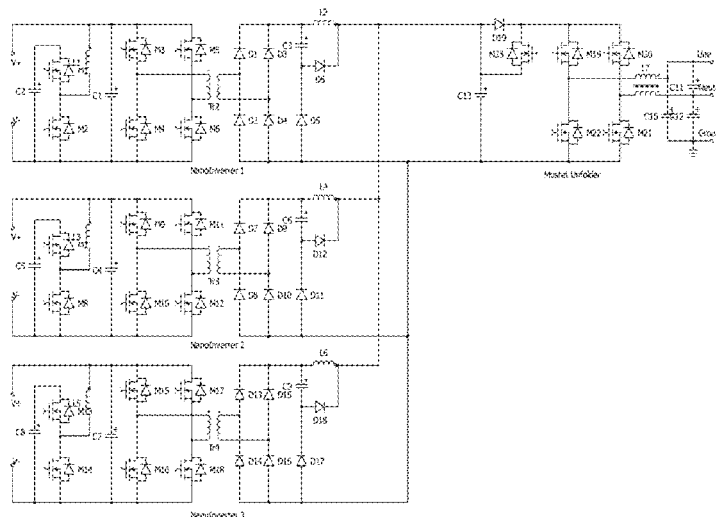
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(57) **ABSTRACT**

An inverter device has an active ripple cancellation boost circuit being configured to a DC source from a plurality of solar cells and configured to filter an AC current ripple back to the DC source and boost the DC voltage to an intermediary 12-15 voltage range. The device has a wave shaper circuit comprising a phase shift zero voltage switching full bridge circuit and a rectifier energy recovery circuit, the phase shift zero voltage switching full bridge circuit configured to shape the DC source to a half wave rectified 120V to 240V waveform. The device has an analog mixed signal controller module configured to generate a PWM waveform and synchronize the rectified waveform to a grid voltage.

18 Claims, 13 Drawing Sheets



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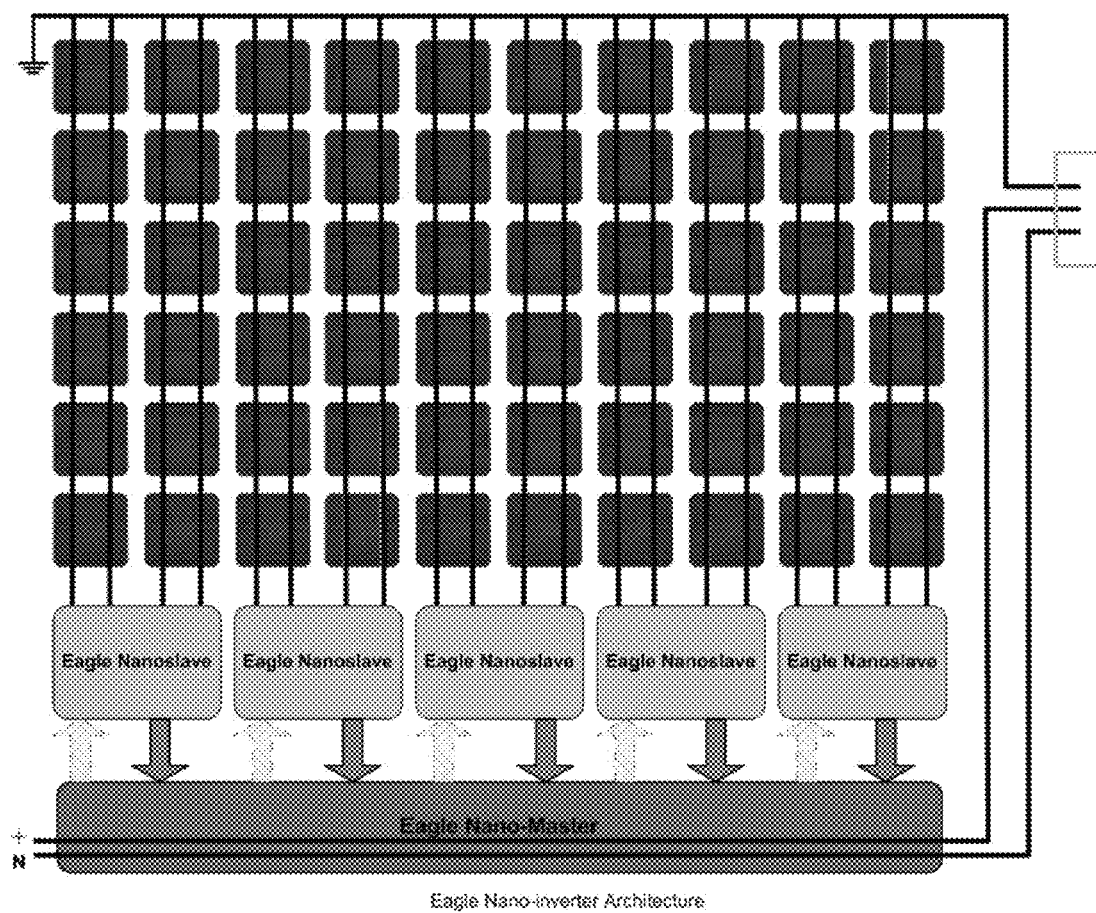
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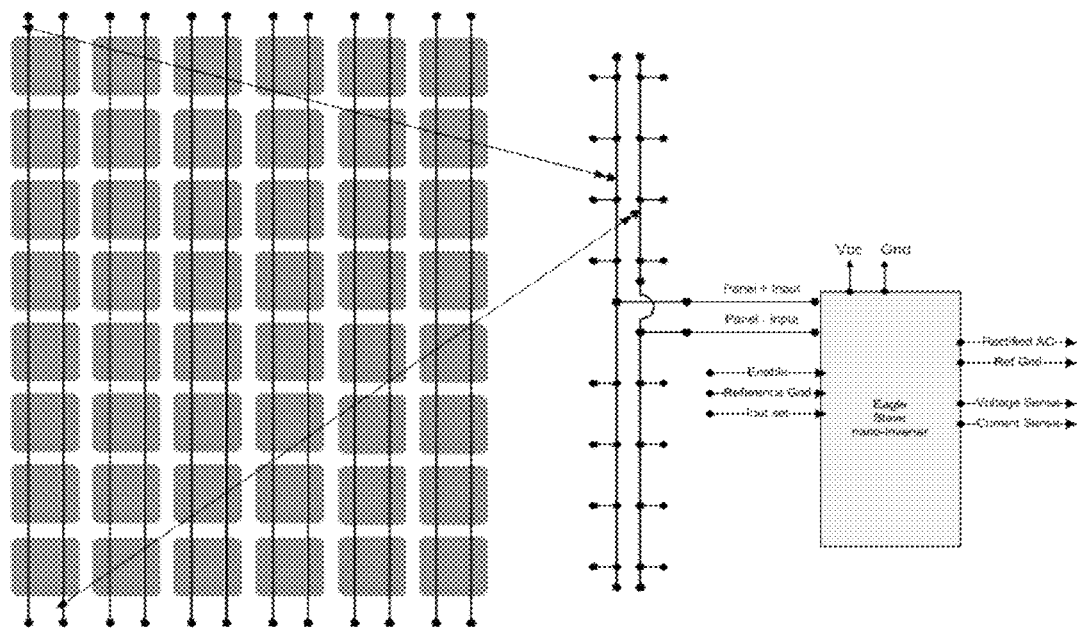
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**FIGURE 1**



mPowerSolar Inc. - The back plane and the slave nano-inverter

FIGURE 2

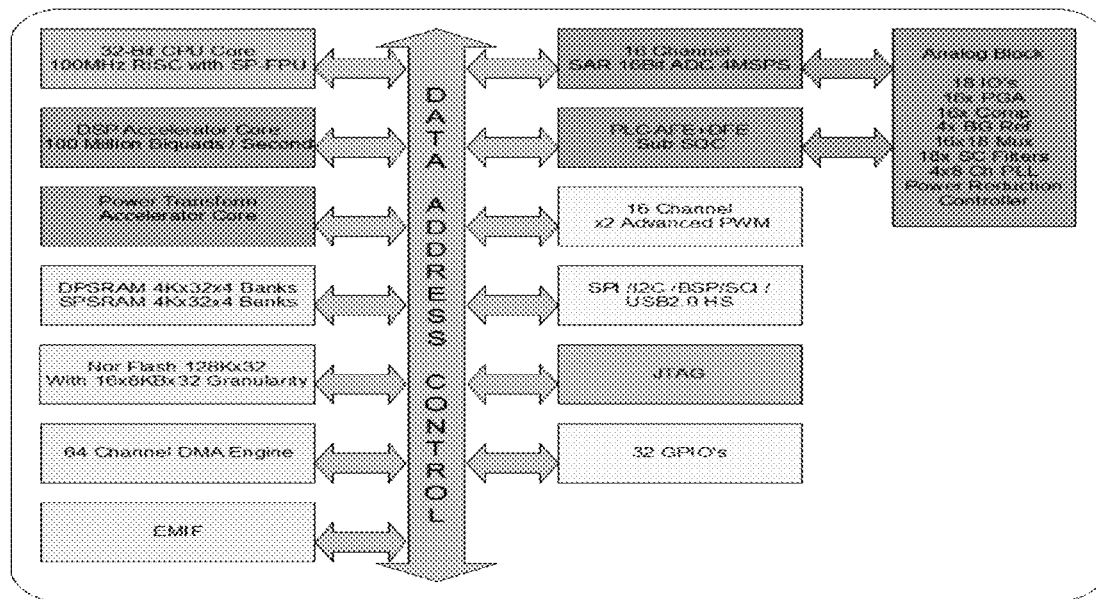


FIGURE 3

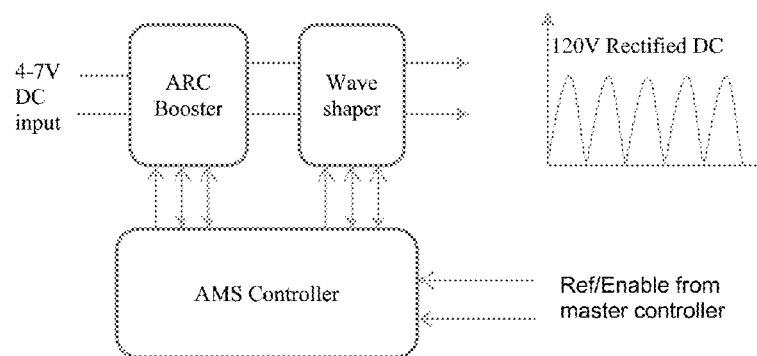


FIGURE 4

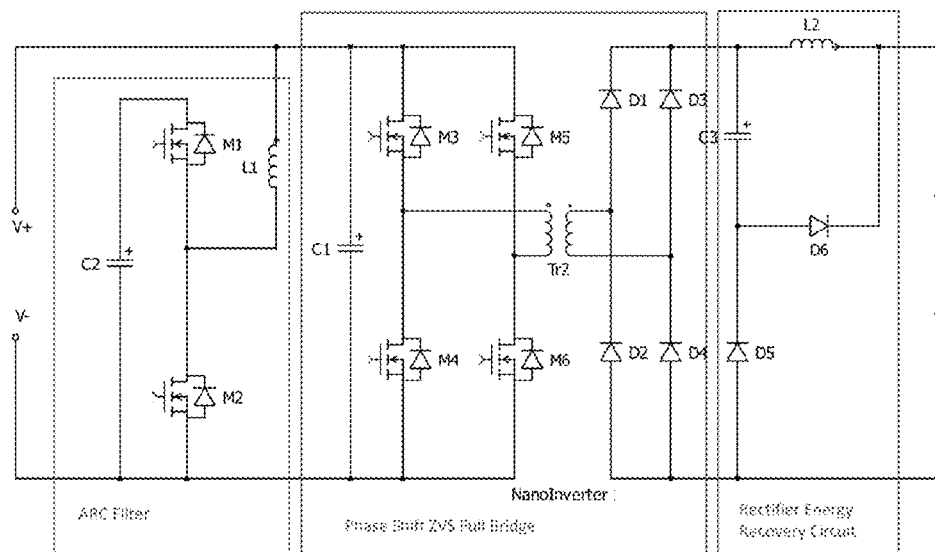


FIGURE 5

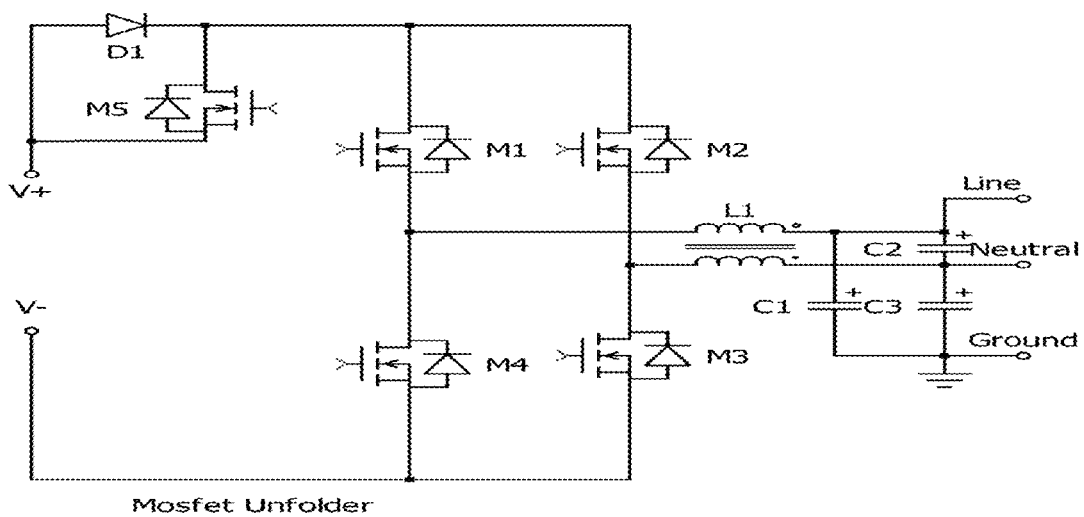


FIGURE 6

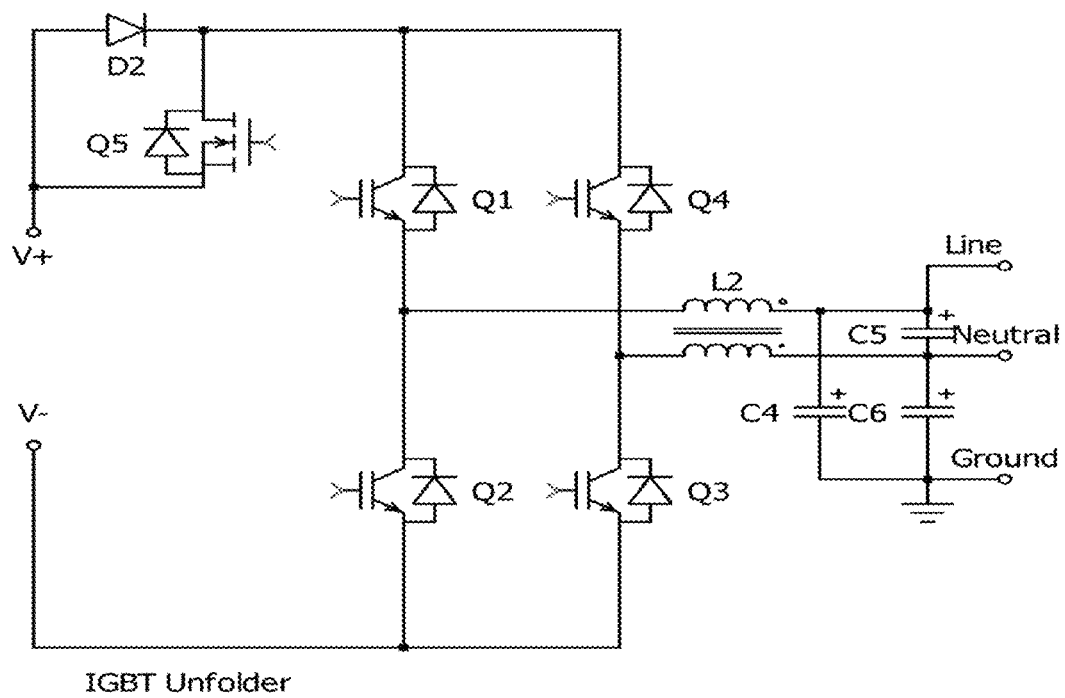


FIGURE 7

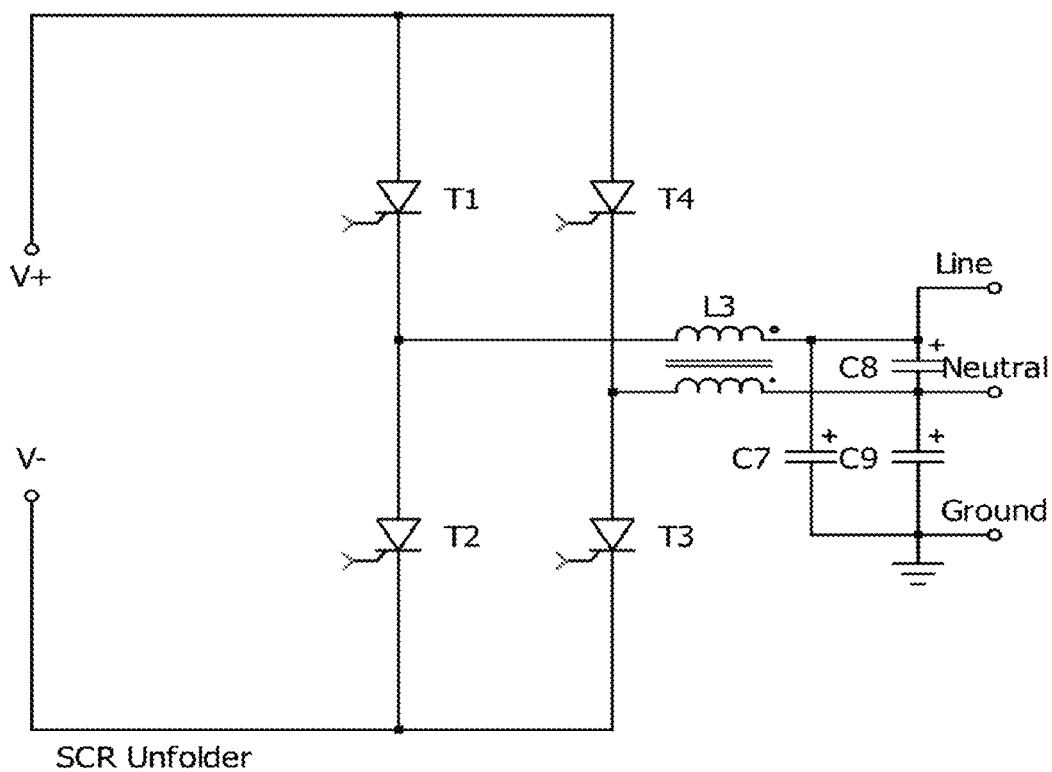


FIGURE 8

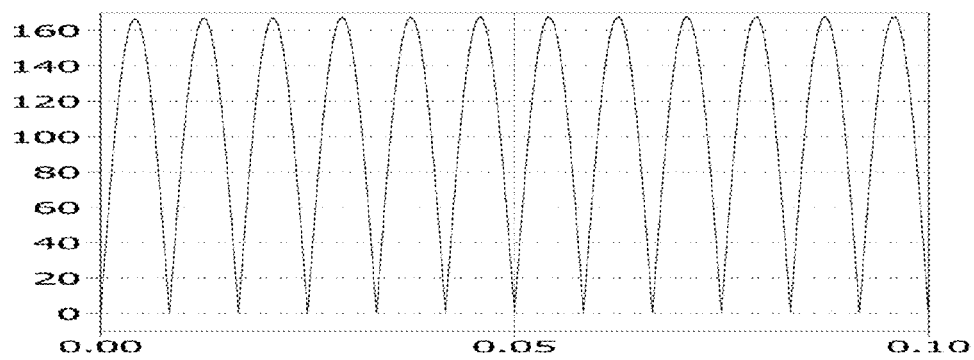


FIGURE 9

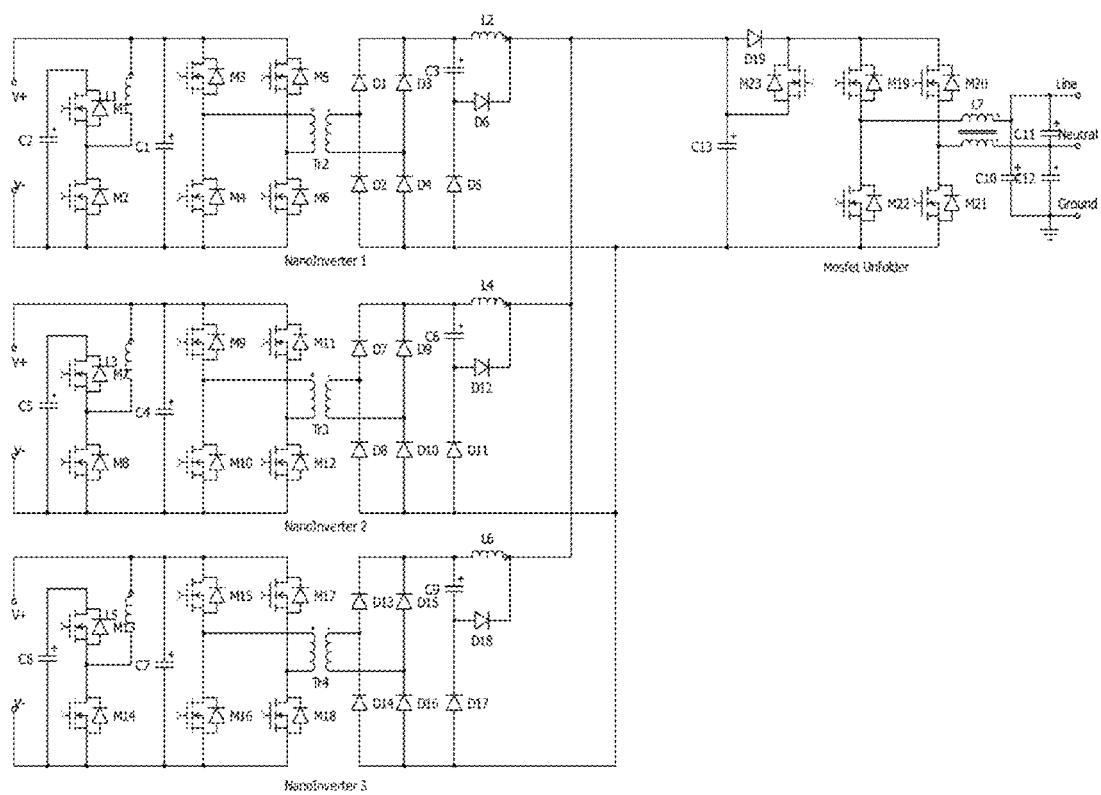
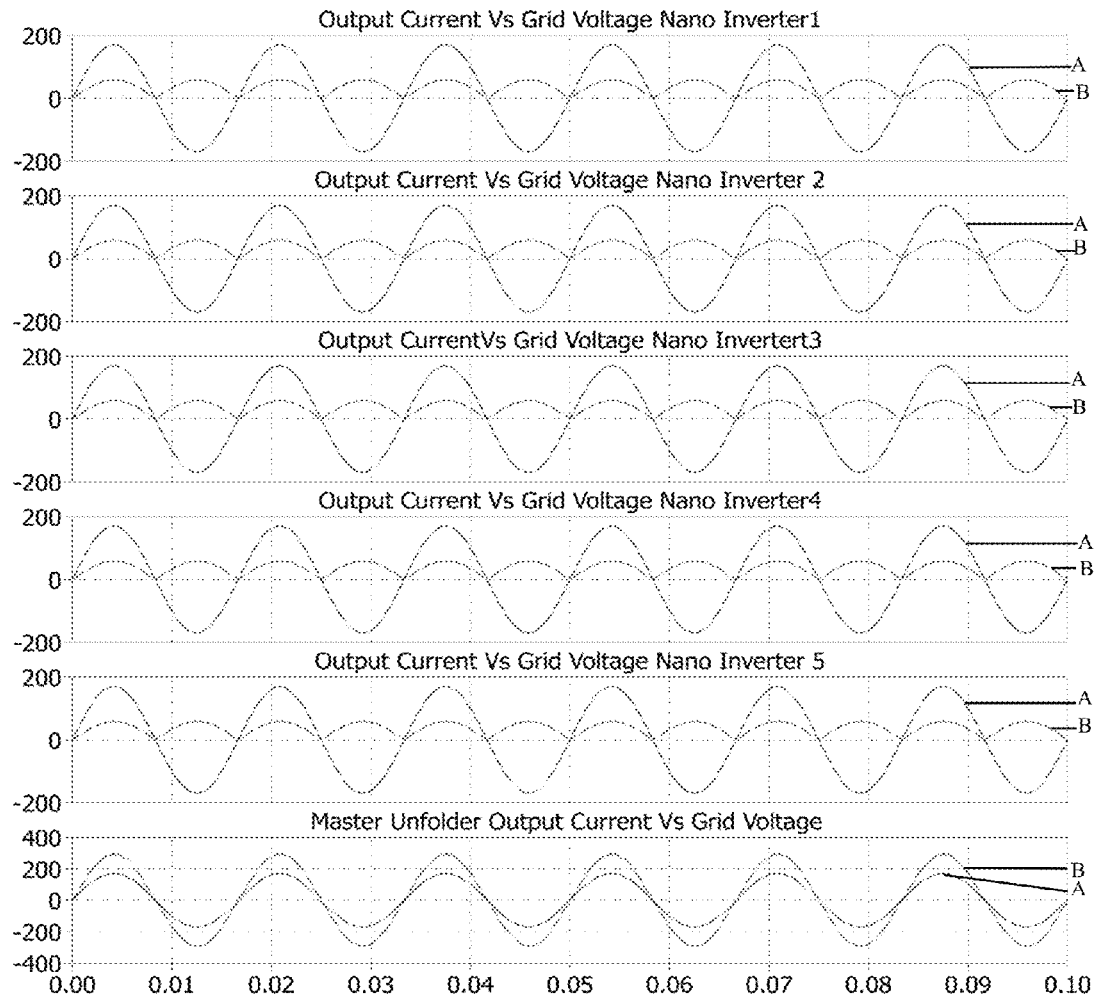


FIGURE 10



Legend: 'A' waveform is the grid Voltage. 'B' waveform is the 100x Current Waveform.

FIGURE 11

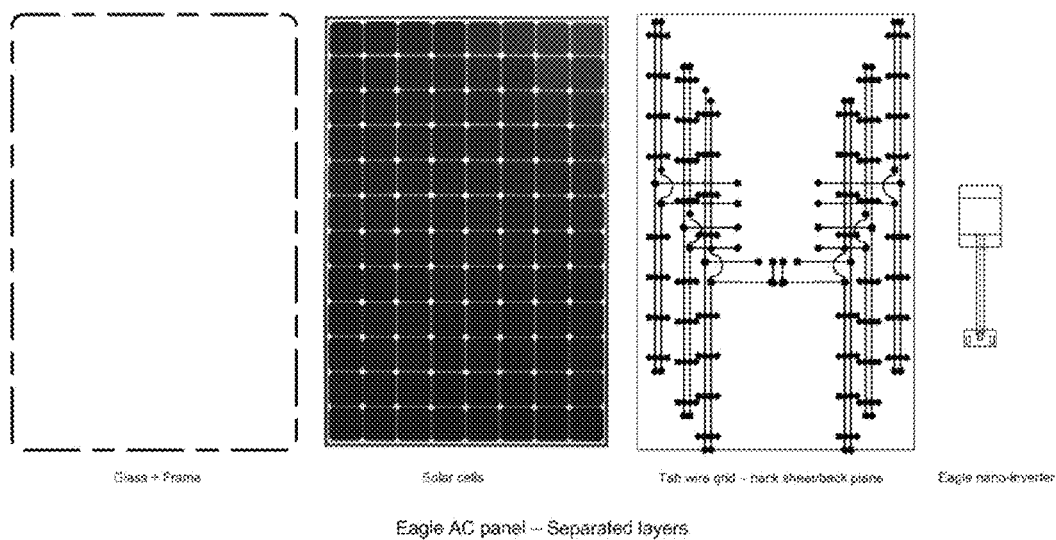
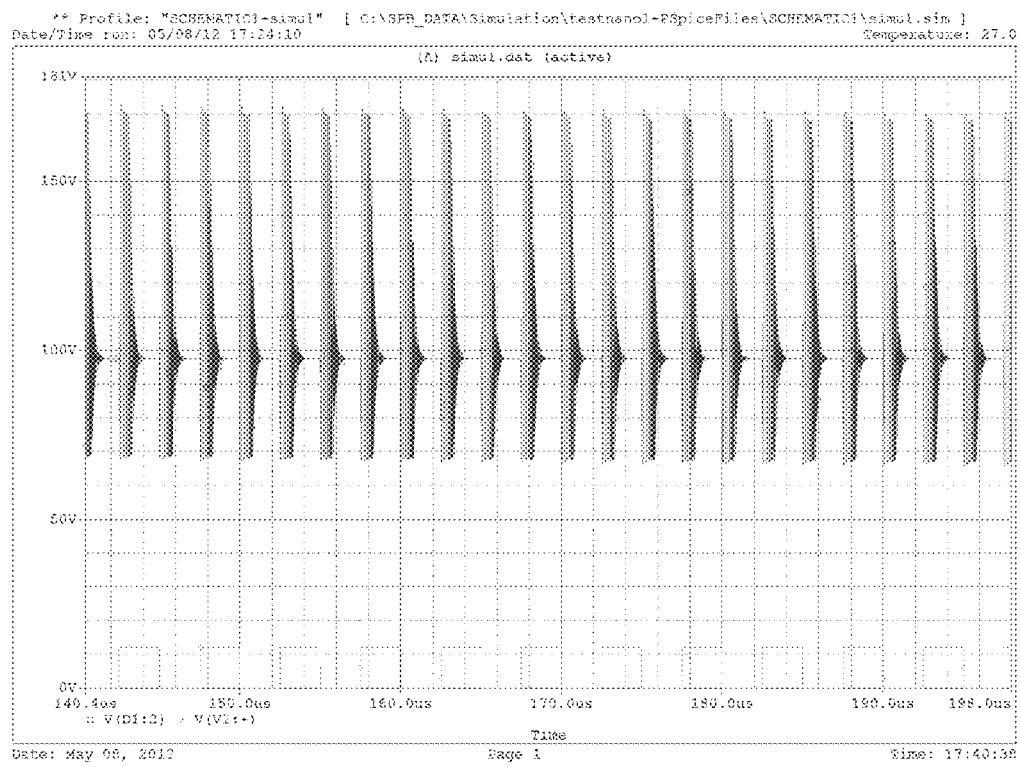


FIGURE 12

**FIGURE 13**

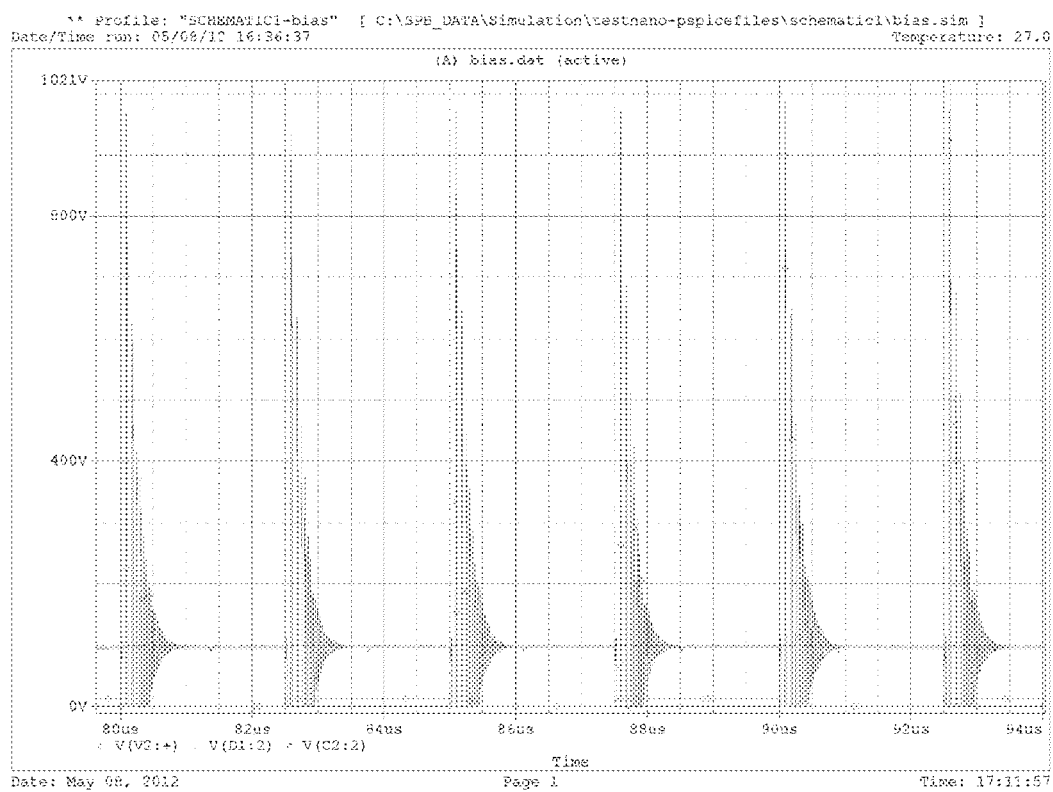


FIGURE 14

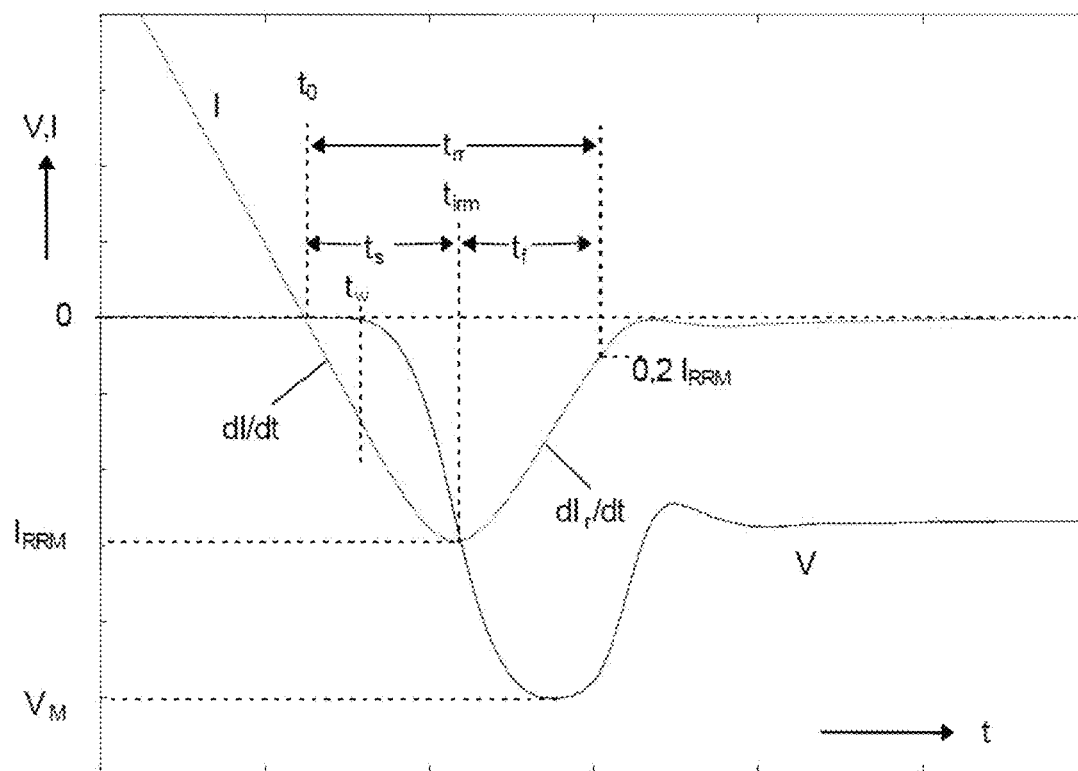


FIGURE 15

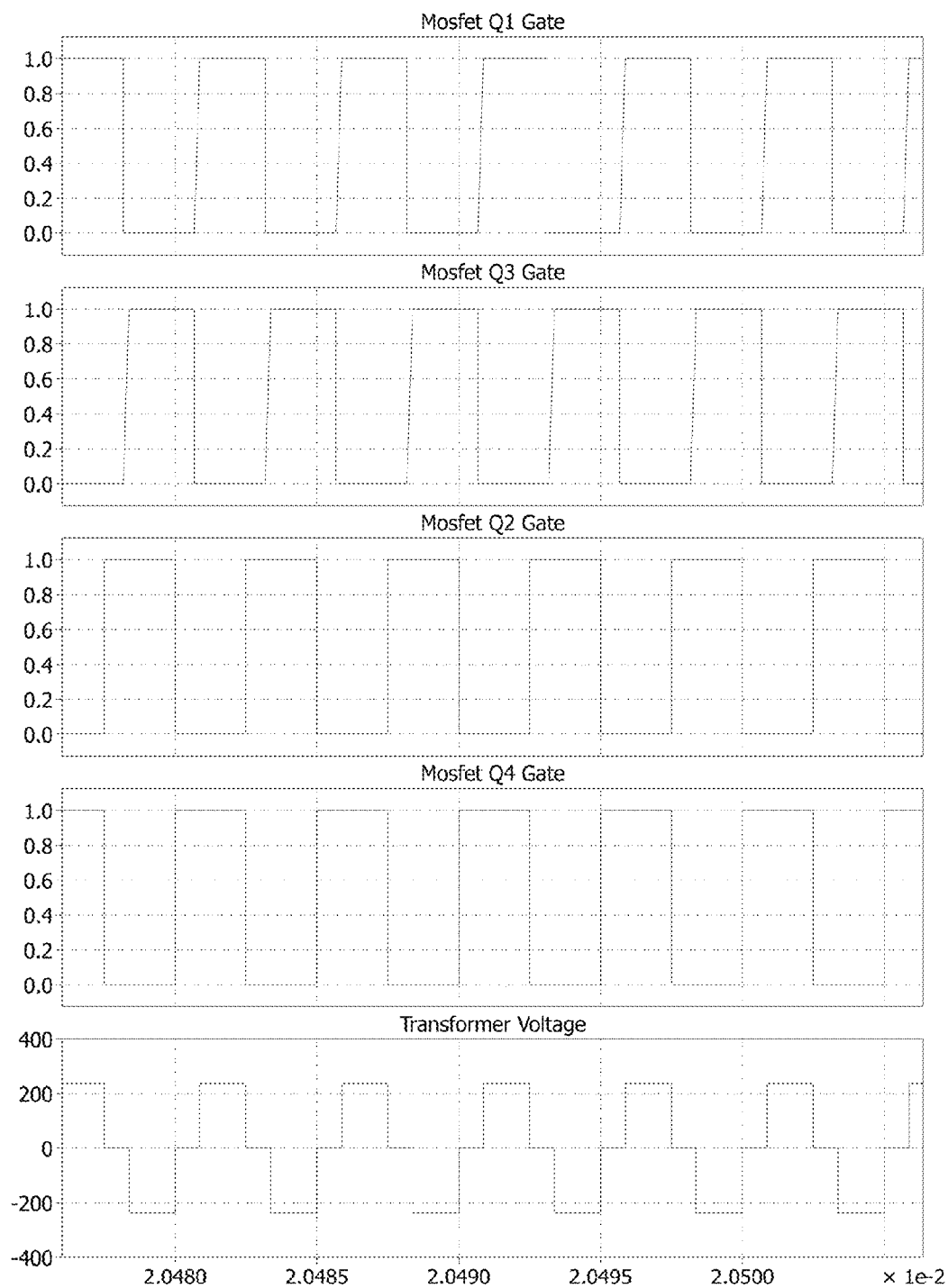


FIGURE 16

SOLAR INVERTER

BACKGROUND OF THE DISCLOSURE

The present disclosure generally relates to integrated circuits. More particularly, the present disclosure provides a method and system for an inverter device configured for a solar module. Merely by way of example, the inverter device can be coupled to a backplane of a solar module, including a plurality of solar cells. Of course, there can be other variations, modifications, and alternatives.

Since the discovery of the photoelectric effect, solar inverters have been designed to convert direct current (DC) electricity produced by solar cells or panels into alternating current (AC). The circuits termed inverters originally refer to the process of constantly inverting the incoming signal from a DC source have been performing the DC to AC conversion from watts to megawatts. Since the resurgence of the PV solar panel technologies in the early 2000's, inverters have become the point of focus as they defined the cost, performance and reliability of solar installations. Clubbed with other components as part of the Balance-of-System (BOS) components the inverter plays a significant role in defining the lifetime of the installation.

As an example, the US Department of Energy has launched the SunShot™ initiative to achieve the goal of an installed cost of \$1/watt (DC) for solar systems for residential, commercial and utility-scale photovoltaic (PV) solar installations. With panel costs rapidly falling, the inverter, BOS costs and installation costs have been the focus for the PV industry. In addition the lower system efficiencies (Solar-panel to grid/end point of load), hovering around 80%, have been an area of concern as they contribute to significant capital expenditure and O&M costs. Efficient power conversion topologies that would lower the cost, improve system efficiency and performance have been sought to achieve the goal of grid parity for Leveraged cost of electricity (LCOE) for PV Solar power.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified top view diagram of a solar module comprising a plurality of cells and associated inverters according to an embodiment of the present disclosure.

FIG. 2 is a simplified top view diagram of a module backplane coupled to a slave inverter according to an embodiment of the present disclosure.

FIG. 3 is a simplified diagram of a master chip module according to an embodiment of the present disclosure.

FIG. 4 is a simplified diagram of a slave chip module according to an embodiment of the present disclosure.

FIG. 5 is a more detailed of the slave circuit of FIG. 4, including filter, phase shifter, RERC, and boost circuit (including phase shifter and RERC) according to an embodiment of the present disclosure.

FIGS. 6, 7, and 8 are examples of inverter circuits according to an embodiment of the present disclosure.

FIG. 9 is a waveform derived from a slave circuit according to an embodiment of the present disclosure.

FIG. 10 is an overall diagram of a master circuit coupled to a plurality of slave circuits according to an embodiment of the present disclosure.

FIG. 11 illustrates each of the voltage and current wave forms from each of the slave circuits and an aggregation of each of the voltage and current wave forms according to an embodiment of the present disclosure.

FIG. 12 illustrates solar cell elements, including a glass member, a plurality of cells, a backplane, and an inverter according to an embodiment of the present disclosure.

FIGS. 13 and 14 illustrate waveforms with switching voltages across rectifier bridge diodes with and without the RERC circuitry according to an embodiment of the present disclosure.

FIG. 15 illustrates a voltage/current plotted against time for the circuitry of FIGS. 13 and 14.

FIG. 16 illustrates waveforms of a wave shaper circuit according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS OF THE DISCLOSURE

The present disclosure generally relates to integrated circuits. More particularly, the present disclosure provides a method and system for an inverter device configured for a solar module. Merely by way of example, the inverter device can be coupled to a backplane of a solar module, including a plurality of solar cells. Of course, there can be other variations, modifications, and alternatives.

As PV panel increase in rated output power, the notion of running at the Maximum Power Point (MPP) has been a preliminary requirement to maximize the power generation. In addition "stringing" PV panels, which can differ in their MPP points by +/-3-5% usually results in almost all panels being run at sub-optimal power points. Further the effects of shading and soiling, which contribute to higher losses get amplified in string topologies. As a result, central inversion and string inversion topologies have substantially lower system efficiencies. These topologies with advantages of price and reliability prove to be costly in the long run. For most financed PV projects, the higher economic cost of central inversion topologies is preferred owing to these advantages sacrificing system performance. A significant short-coming of the central inversion topologies is their inability to aid O&M through panel level monitoring and reporting. String designing, layout optimization, BOS component costs and EPC costs are significantly higher for central inversion topologies which are usually ignored while calculating the utility of such topologies.

Distributed converters or micro-inverters on the other hand perform the task of inversion at the panel-level enabling the system to deliver the optimal efficiency in all weather conditions. Since the output of each micro-inverter is a grid synced AC power at the desired voltage, micro-inverters are usually daisy chained to aggregate the AC current from each panel. Micro-inverters eliminate mis-match losses, suboptimal power point losses and significantly lower the effect of shading and soiling losses. In addition they bring the benefits of panel monitoring and reporting to aid O&M. Micro-inverter performance against other topologies is as shown below.

In an example, certain challenges face distributed power converters. Micro-inverter solutions have been challenged on the aspects of cost and reliability. Several first generation micro-inverter solutions have been perceived as significantly costly and unreliable. Reliability concerns severely hinder the adoption of micro-inverters in commercial and utility-scale segments where field failures would result in significant costs to repair and replace. Most micro-inverter companies however have been producing HALT/ALT and field trial data to prove their reliability. Concerns of adopting a "new technology" with significant cost impact is expected to abide within the next couple of years as more field performance data becomes available. Micro-inverters, while cost effective at

the system-level, are often termed the higher cost alternative when inverter-to-inverter prices are compared.

As micro-inverters gained prominence in the PV solar market initially in the residential and small commercial (<15 KW) PV installations, the notion of developing an integrated AC panel that significantly reduces the cost while significantly lowering installation costs and remaining BOM costs is being pursued jointly by major panel manufacturers and micro-inverter companies. This approach still allows for clear distinction of liability between the panel and the micro-inverter in case of a failure. The notion of an integrated solution however suffers from major disadvantages as there are no significant cost, performance and reliability benefits. There has been a significant discussion in the industry as to what exactly constitutes an "AC Panel" and how it can achieve the \$1/watt cost to normalize PV solar LCOE by the end of the decade. In addition these approaches keep the solution at the system level, slightly out of the reach of custom ASICs that can lower the cost significantly while improving reliability. [0022] In an example, the AC panel desirably focuses on the core issues of cost and reliability while striving to improve the performance of the "AC Panel". In addition the fundamental power conversion architecture needs to provide for custom ASICs with lagging processes to significantly lower cost and much higher reliability. The Eagle—Black plane integrated inverter AC panel described in the next chapter is the next generation AC panel technology that would significantly alter the solution landscape for PV Solar installations.

In an example, the present inverter device can be integrated into the back plane of a solar panel to overcome the challenges facing the AC panel technology. The present panel is defined by a holistic approach to the AC panel solution with cost, reliability and performance being tackled simultaneously in the product design. As observed earlier cost reduction of inversion technology is only possible through custom ASIC which are generally difficult for power electronic circuits. Multi-chip modules with expensive packaging technologies are usually the chosen avenue to develop custom power circuits at lower cost. The present panel technology however relies on an innovative Master/Slave architecture to implement "nano" inversion on the DC power generated by a group of cells in the PV panels. Since the power handled by the cells is lower the present AC panel, comprises of breakthrough DC-DC boost circuit that achieves over 20x-40x voltage boosting at higher than 98% efficiency. In addition the circuit uses innovative "energy recovery circuits" to eliminate the use of expensive SiC diodes in the output bridges and replace them with inexpensive Schottky diodes. This innovative circuit also enables the entire solution to be packaged in an ASIC with lagging edge IC fabrication processes delivering superior performance at a fraction of the cost.

The present panel technology solution has a "Master" control and communication ASIC that works in tandem with up to 24 "Slave" inverter ASICs. The master/slave AC panel topology is a highly scalable solution that can be implemented in PV panels of 60 cells, 72 cells or 90 cells to deliver 120V/240V/277V AC panels. These AC panels would be independently grid-tied to enable installation all the way from a 300W-1MW. As each AC panel comes completely integrated with a grounded AC output, the system assembly and installation process becomes completely simple and extremely safe.

The Master/Slave topology consists of one single Master ASIC controlling the Slave ASICs, which are connected to a group of cells in the AC panel. This is achieved through the "Back Plane" which is essentially a grid array of cell connections that optimizes their placement to group the cells. Each

cell group is expected to deliver at least 4-7V DC at the input of the Slave ASIC. The details of the "Back Plane" are explained in the following section.

The AC panel master/slave topology reduces the need for expensive magnetic components as well as energy storing capacitors. The Master ASIC of the AC panel to monitor the grid for the requisite voltage and frequency parameters and enables and disables the slave inverters accordingly. Cells in the panel can be separated into arrays of 10 or 12 (depending on Poly silicon/Mono crystalline/Thin film cells) into a custom designed "Back Plane" that optimizes the routing length from each group of cells to the input of their corresponding Slave inverter. As the number of cells in a group is determined by the requisite voltage input to the Slave inverter, AC panels of various output power are possible. As each Master ASIC can control up to 12 Slave inverters, AC panels ranging from 240W-1.4 KW can be designed. The limitation on panel size would then be determined by the mechanical constraints than electrical constraints. In addition, optimal cost savings could be achieved around the 640W systems with 277V outputs, which would enable 480V 3-phase systems.

FIG. 1 is a simplified top view diagram of a solar module comprising a plurality of cells and associated inverters according to an embodiment of the present disclosure. As shown in the Figure above, the present plane inverter architecture breaks the inversion process into DC boost with MPPT and generation of a 120V/240V/277V rectified DC waveform from each group of cells in the panel and aggregating their currents in the AC un-folder circuit controlled by the Master ASIC. The optimization of the cell placement is achieved by the custom designed "Back Plane" enables the Slave inverter to have a extremely low profile planar DC boost transformer integrated along with the ARC filter inductor. The DC boost circuit described in the following sections, achieves 20x-40x boost using a proprietary switching technique that achieves "zero voltage" switching at >200 KHz switching frequencies. The Slave inverter also senses the voltage and current of the panel group to run a cell-group level MPPT optimizing the power from each cell group. This enables the inverter powered AC panel to deliver significantly higher performance than AC panels integrated with micro-inverters. The encapsulation of all critical circuits into custom ASIC significantly improves the reliability of the AC panel, well beyond the customary 25 years. This higher reliability also comes with increased performance and substantially lower cost.

FIG. 2 is a simplified top view diagram of a module back-plane coupled to a slave inverter according to an embodiment of the present disclosure. The "Back Plane" of the AC panel is custom designed grid arrangement that groups the cells on the panel into groups driving the power circuit of a Slave inverter. The "Back Plane" (BP) in an integrated part of the electrical circuit as it plays a significant role in optimizing the cell layout.

The BP allows for minor improvements in the integration of the Master/Slave inverters by choosing the cell groups for each Slave inverter. The physical proximity of each cell group to the Slave inverter enables lower cost of tab wires while providing for "nodes" on to which the cells can be directly placed during panel assembly. The BP circuit is an addition plane layer hooked to the main inverter PCB which holds the Master/Slave ASICs. The BP shape and layout are determined by the characteristics of the cells being used for the AC panel. The number of nodes could be much smaller for a "Thin film" panel as most of the individual cells are combined in parallel, than that of a "Poly-silicon panel" where in most of the individual cells are connected in series. As a result the nodes

on each individual cell branch are defined by the cell material and needs to be optimized based the desired cell output power and voltage. The aim of the BP is to ensure optimal cell grouping so that the input DC voltage from them is at least 4V. The BP also needs to ensure minimal losses on the tab wires by minimizing their lengths before reaching the input of the Slave inverters.

FIG. 3 is a simplified diagram of a master chip module according to an embodiment of the present disclosure. As shown, the master chip module is a master ASIC. The Master ASIC hosts the central control part of the AC Panel. The Master ASIC has the following features.

1. Controls up to 24 Slave inverters and the integrated AC un-folter.
2. Control algorithms for both Grid-Tie and Off-grid Applications with internal sync.
3. Check for IEEE1547/UL1741 Grid Conditions and enable/disable the power production of the Panel on an abnormal grid/load or low power condition.
4. Control the current output of each of the Inverter and enable/disable the Slave inverters in event of an abnormal grid/load condition.
5. Absolute and pre-emptive control on what is put out on the grid side/load side of the inverter.
6. Monitor the individual Inverter power production as well as cumulative power production of AC panel at the output.
7. Produce Proportional reference rectified grid Voltage for the Slave Control ASIC to produce 120/240/277V RMS Rectified Grid Waveform.
8. Synchronize the output un-folter to the incoming grid voltage or load side commutation to produce a clean sinusoidal AC waveform with minimal THD.
9. Communications on Wired/Wireless physical layers to any central data collection system.

In an example, the Master ASIC measures the Voltage and Current signals output from each of the Slave inverters and produces a proportional MPPT set point for each of them. An architectural block diagram of the Master ASIC is as shown.

The Slave ASIC is the Power Production Control ASIC of the Inverter for a given group of cells on the panel. It receives its DC input from a serial or parallel group of cells. The Features of the Slave inverter ASIC are as follows.

1. Monitor the cell group Voltage and Current.
2. MPPT Control the cell group Current/Voltage to ensure that they operate at the MPP point.
3. Collate the Current/Voltage/Temperature Data for monitoring & reporting through the Master ASIC.
4. Produce a Rectified Sine Waveform for the output un-folter bridge at 120V/240V/277V as desired by the AC panel configuration.
5. Maintain a high quality low THD output rectified Sine Waveform for grid interconnection or load side commutation by the master ASIC.
6. High speed precision Mixed Signal Control loop to track the incoming reference signal from the master ASIC.
7. Work in the Average Current mode controller for Grid Tied Operation and Voltage Mode Peak Current Mode Control for Off Grid Applications.
8. A RISC Processor to have precision control state machines and data collation engines.

FIG. 4 is a simplified diagram of a slave chip module according to an embodiment of the present disclosure. As shown, the Block Diagram of the control ASIC is shown.

FIG. 5 is a more detailed of the slave circuit of FIG. 4, including filter, phase shifter, RERC, and boost circuit (including phase shifter and RERC) according to an embodi-

ment of the present disclosure. As shown, the Booster Stage is the key part of the Slave inverter ASIC that enables 20x-40x voltage boost at high efficiency. In addition this Boost converter circuit is designed to use low voltage MOSFETs, which enable the encapsulation of the power circuit in a lagging edge process technology. The cost reduction is further achieved through the use of inexpensive Ultrafast Silicon PN Junction diodes in place of SiC diodes and an innovative "Rectifier Energy Recovery Circuit" minimizes the losses delivering greater than 98% efficiency. The Boost circuit consists of the 3 stages show, above which are described in detail below.

Phase Shift Full Bridge Converter

The PSFB (Phase Shift Full Bridge) Converter works with a constant dead time lagging phase leg average current mode control system. The PSFB and the RERC together use the Magnetizing inductance of the transformer along with the Primary and Secondary parasitics of the transformer to soft switch the primary side switching components (M3, M4, M5, M6) in a fashion that the ZVS operation is valid for any duty cycle. Regular designs involving the PSFB use the leakage inductance of the transformer or an additional inductor in the primary path to achieve ZVS on the primary side switching components. The main advantage of this circuit is that the Diodes D1 thru D4 which rectify the output of the transformer does not freewheel with the Inductor. Hence full Discontinuous Conduction Mode (DCM) is achieved on the rectifier Diodes.

The DCM mode of operation is crucial for the transformer to cut off at a predefined interval exposing the magnetizing inductance to the primary side components for a Zero Voltage Switching during dead times between M3, M4 and M5, M6. Zero Voltage Switching of primary side components is highly desirable as these components can be switched at a much high frequency thereby reducing the size of the transformer, inductor and capacitors needed in the circuit. The Slave inverter can effectively be built with integrated magnetic switching at >250 KHz to about 2 MHz limited with the availability of Ferrite Materials.

The unique feature of the circuit is to use the primary magnetizing inductance which is lossless to actually free-wheel the primary part of the circuit to reduce the switching losses of the Converter considerably to an insignificant level and reduce the common mode conduction loss of the primary side switching components and use minimum parasitics on the switches to achieve ZVS Commutation. The energy storage in the transformer becomes very less owing to a higher inductance value used for ZVS commutation and nullifies the need for a leakage inductance thereby tightly coupling the Primary and Secondary windings of the transformer with a high coefficient of coupling. The Primary Side Switching circuit operates satisfactorily in ZVS mode for a Primary Leakage Inductance in the range of 0-10% of the Primary Magnetizing inductance of the transformer indicating that the leakage inductance has insignificant role in the commutation of the ZVS transition of the Primary Side Switching Components.

Rectifier Energy Recovery Circuit

The Rectifier Energy Recovery Circuit (RERC) is a crucial part of the PSFB Circuit to operate in the ZVS region. The RERC removes reverse recovery charge if any on the rectifier diodes (D1 thru D4) thus enabling the use of regular inexpensive Silicon PN Junction diodes against expensive high voltage SiC Schottky Diodes.

The RERC recovers the junction energy of diodes D1 thru D6 in to the capacitor C1 and then transfers the energy to the

output thus making the diodes D1 thru D4 behave like a majority carrier device as a schottky diode.

The RERC also free wheels the inductor making D1 thru D4 always stay in DCM irrespective of the output Power Level. Making Diodes D1 thru D4 to stay in DCM is crucial for the Converter as this nullifies the switching losses to an insignificant value and hence the Converter can be operated at a significantly higher frequency reducing the Inductive and Capacitive components in the circuit thereby reducing the form factor and size of the circuit considerably.

ARC Filter Stage

The Active Ripple Cancellation (ARC) Filter cancels the DC Current Ripple found on the input Solar Panel Voltage. M1 and M2 switches operate on a principle of a bidirectional DC-DC Converter. The ARC Filter Charges Capacitor C2 to a stipulated voltage during low conduction states of the PSFB and will discharge the capacitor during high conduction states of the PSFB Converter.

The ARC filter operates the switches in a fully Zero Voltage Switched Operation using a Constant Dead-time Average Current Mode Control. The ARC Filter intends to replace Aluminum Electrolytic Capacitors with a high reliability Metal Film or Ceramic Capacitor of a lower capacitance Value.

The Capacitor C2 is fully utilized on the Voltage Scale between Vin and Vmax Rating of the Capacitor. The ARC Filter filters out the 120 Hz/100 Hz Line frequency ripple introduced by the PSFB minimizing the current ripple seen by the Solar Panel.

AC Un-Folder Circuit

The AC Un-Folder Circuit is critical for this implementation. The Aggregated power of each of the Nano Inverter Boost Circuit is available on the AC un-folder Input V+/V-. Since the output of the boost circuit is a rectified sine wave, the Un-folder circuit converts the incoming rectified sine wave to line frequency AC sine wave. In principle, the un-folder circuit has to prevent any rectified sine waveform from the line to enter into the Boost Circuit Output when the boost circuit is not producing any power. Though the un-folder circuit is hard switched, the switching losses are negligible due to the low switching frequency which is usually the line frequency (50/60 Hz).

In the following sections, various schemes of implementing the AC Un-folder are specified, which are also referred to in FIGS. 6, 7, and 8.

MOSFET Un-Folder

In this Scheme, the Mosfets M1, M2, M3, M4 form the unfolding commutation circuit. When the voltage between Line and Neutral is positive, M1, M3, M5 are on and when the Line and Neutral is negative, M2, M4, M5 are on. The Line Filter comprising of L1, C1, C2, C3 filter out the switching transient effects from the Unfolding Circuit. Diode D1 forms a Reverse Blocking Diode which does not allow the body diode rectification to enter into the boost circuit output when the system is not producing any power. To reduce the losses of the Diode D1, Switch M5 is used, switch M5 is on when there is power production from the system. This Un-Folding Scheme allows for a low conduction loss implementation in voltages up to 250V Rms. The Un-Folder Dead time of this implementation can be less than a 200 ns making the Un-Folder output a very clean Sine wave of less than 2% THD. Since the output switches can be controlled, the system can be shut off at any point on the line cycle.

IGBT Un-Folder

In this scheme, the IGBT's Q1, Q2, Q3, Q4 form the unfolding commutation circuit. When the voltage between, Line and Neutral is positive, Q1, Q3, Q5 are on and when the

Line and Neutral is negative, Q2, Q4, Q5 are on. The Line Filter comprising of L2, C4, C5, C6 filter out the switching transient effects from the Unfolding Circuit. Diode D1 forms a Reverse Blocking Diode which does not allow the body diode rectification to enter into the boost circuit output when the system is not producing any power. To reduce the losses of the Diode D1, switch Q5 is used, switch Q5 is on when there is power production from the system. This Un-Folding Scheme allows for a low conduction loss implementation in voltages between 400V up to 600V Rms. The Un-Folder Dead time of this implementation can be less than a 500 ns making the Un-Folder output a very clean Sine wave of less than 3% THD. The system will be rugged as the devices Q1, Q2, Q3, Q4, will have a short circuit rating for a period of 10 us. Since the output switches can be controlled, the system can be shut off at any point on the line cycle.

SCR Un-Folder

In this Scheme, the SCR's T1, T2, T3, T4 form the unfolding commutation circuit. When the voltage between, the Line and Neutral is positive, T1, T3 are on. When the Line and Neutral is negative, T2, T4 are on. The Line Filter comprising of L3, C7, C8, C9 filter out the switching transient effects from the unfolding circuit. Since SCR's are unidirectional conduction devices, the system does not require a blocking diode. This un-folding Scheme allows for a low conduction loss implementation in voltages between 100V up to 600V Rms. The un-folder dead time of this implementation can be less than a 100 us making it output a Sine wave of slightly less than 5% THD. The system will be rugged as the devices T1, T2, T3, and T4 will have a short circuit rating for a period of 10 us. Since the output switches can be controlled on and not off, the system can be shutoff only at the zero cross of the line cycle.

The key feature of the AC Panel remains the integration of the power generated from each of the Slave inverters by the Master. The integration and control aspect of the AC panel remains critical as power aggregation at small currents is quite difficult. The Master/Slave architecture of the AC panel has 2 architectural features in place to enable power aggregation with simple control algorithms.

1. Reference synced rectified DC output waveform at uniform voltage from Slave inverters
2. Synced current wave form matching the reference signal generated by Master from the Slaves

For instance to generate a 120V AC at the output of the AC un-folder the Master would set the rectified DC voltages of the Slave inverters at 169V RMS.

FIG. 9 is a waveform derived from a slave circuit according to an embodiment of the present disclosure. The output voltage waveform from each of the Slave inverters for a 120V AC output is as shown.

FIG. 10 is an overall diagram of a master circuit coupled to a plurality of slave circuits according to an embodiment of the present disclosure. In addition to the voltage set point, the reference sync signal, which would be a low voltage stepped down grid voltage of 2.5V p-p for grid-tied application and master generated 2.5 Vp-p rectified sine wave for off-grid application, ensures an identical voltage waveform from each of the Slave inverters. The Slave inverters further generate a matching current waveform depending on the current set point provided by the Master corresponding to their MPP points. These reference points also help the Master enable/disable the Slave inverter in less 10 us, to comply with the anti-islanding requirements for various safety standards. In conjunction with the reference signal, voltage set point and current point a fool-proof shutoff can be implemented in the Slave inverters with relatively simple control loops. At the

same time, the steady state run time performance is made flawless with these reference signals from the Master, making a the control loops for the Slave absolutely rudimentary. It is important to note that the MPP points for each of the Slave inverters is determined by the Master which has much higher compute power than the AMS controllers in the Slaves. The Master samples the current and voltage values from each of the Slave devices at the beginning of each AC cycle to determine their corresponding set points. The following figure shows the circuit of the interconnection of the Slave inverter outputs aggregated to feed the AC un-folider (MOSFET un-folider shown here). The parallel interconnection is possible due to the identical waveforms generated from each of the Slaves. The current waveform generated from each of the Slaves is also a rectified sine wave, synced up to the reference signal provided by the master. The aggregation of the current waveforms at various amplitude levels does not have any bearing on the output THD, as they are phase aligned and frequency correlated. The input of the AC un-folider with an active MOSFET circuit ensures that the aggregated rectified DC current and voltage waveforms are filtered to ensure a smooth sine wave. The AC un-folider circuit can thus be a simple commutation circuit that converts the rectified DC voltage and current waveforms into the desired AC waveform at requisite line frequency. The output line filters are designed to provide 120V/240V/277V single-phase or 240V split phase AC outputs directly from the panel. This simplifies the output AC cable design which can be any regular grounded AC connector with 15A current rating. The following figure illustrates the independent current wave forms from the Slave inverters plotted against the reference voltage waveform. The last waveform in the figure shows the aggregated AC panel voltage and current waveform.

FIG. 11 illustrates each of the voltage and current waveforms from each of the slave circuits and an aggregation of each of the voltage and current wave forms according to an embodiment of the present disclosure. Note: Legend: 'A' waveform is the grid Voltage. 'B' waveform is the 100× Current Waveform.

FIG. 12 illustrates an AC module or panel, including glass/frame, solar cells, backplane, and inverter according to an embodiment of the present invention. As shown, the AC panel overcomes challenges limiting the wide spread adoption of AC panels in solar PV installations. In each of the three significant aspects—cost, reliability and performance, the AC panel solution fares far better than current solutions. Elimination of junction box diodes saves 2-3% of power loss straightaway in this example. Each cell group performing at MPPT significantly lowers soiling losses making the solar panel can work even on partially shaded conditions providing a higher MPP performance over a regular micro-inverter/central inverter under the same conditions. Optimization or improvement of cell group performance improves the overall MPP performance by 5-10% in an example. Slave inverters deliver greater than 98% efficiency with PSFB and RERC circuits. Overall efficiency higher than 97% from the panel delivering AC in this example.

ZVS switching delivers high efficiency even for 240V/277V systems with about 40× boosting in an example. Overall system performance surpasses the combination of DC Optimizer with Central inverter or regular micro-inverter by about 5-10% depending on conditions. Overall System Efficiency in commercial scale can be improved from 91-93% to about 96%(Limited by AC Cable Design) under field Conditions. In an example, elimination of cable costs lowers AC

panel cost by about 20% in an example. Elimination of enclosure for the inverter eliminates 5% of the cost in an example. Elimination of junction box in the panel saves about \$15. Elimination of DC cable connectors saves about \$7 in an example. Elimination of assembly costs related to Panel and micro-inverter in an example. Combination of back panel and integrated Inverter PCB saves panel costs in an example. Encapsulation of power circuit in a custom ASIC cuts the cost of power circuit by 80% of its discrete solution in an example. Encapsulation of the control and communication ASIC lowers the cost of the Master controller to about 50% of the current discrete solution in an example. Inverter based Master/Slave architecture lowers the cost of magnetic by 50% in an example. Inverter based Master/Slave architecture replaces Metal Film Storage of Line frequency Power with highly inert Ceramic Capacitor lowering the cost by 80% in an example. The solution nears a \$0.12/watt DC installed for Inverter and BOS in an example. Elimination of the DC Ground removes the need for DC GFDI which lowers the BOS Cost by 5% in an example.

In an example, opto-isolators and discrete gate drive circuits are eliminated improving MTBF. Integrated planar magnetic components improve the mean time between failure MTBF and field repeatability and simplifies production. Encapsulation of power circuit on Slave ASIC improves reliability. Encapsulation of control and sense circuits in slave ASIC eliminates discrete components prone to degradation. Elimination of high capacity metal film capacitor with automotive grade ceramic capacitors improves the reliability and power density of the product by a major margin.

Referring now to FIGS. 13, 14, and 15, as shown are waveforms from a full-bridge rectifier circuit at the secondary of the transformer that converts 1666 digital sine wave samples into absolute (only positive pulses) pulses. As a result the diodes switch 1666 time during each sine wave cycle. Part of the energy transferred across the transformer by the PSFB is lost every time a diode in the rectifier bridge switches. The common diode power loss is due to the reverse recovery charge present on the diode at the time of switching. The reverse recovery energy loss (FIG. 15) is given by $V_m \cdot I_{rrm} \cdot t_{rr} / 2$. Refer to the image for the actual loss. As the switching times are high this loss is pretty significant. The Reverse Energy Recovery Circuit, actually adds additional passive elements to snub these losses. An additional capacitor C3 in the snubber circuit is charged during the reverse recovery period and recycled into the output during the time the diode actually conducts. Over a period of 1666 switching cycles 3-4% of power loss could be saved through the RERC circuit. Waveforms with the switching voltages across the rectifier bridge diodes with and without the RERC circuitry are provided by FIGS. 13 and 14.

Referring to FIG. 16, the present wave shaper circuit includes a phase shift full bridge circuit consisting of 4 power MOSFETs coupled to a transformer. The MOSFETs are switched alternatively (upper leg on, lower leg off and vice versa) and the waveforms of the individual legs are phase shifted. The relative phase shift in turning on/off the MOSFETs generates a digital sine wave at the input of the transformer. A series of these digital sine wave generates a half-wave voltage waveform of 120 Hz/100 Hz (for 60 hz/50 hz line frequency) across the inductor at the output of the secondary side of the transformer. The current waveform across the output is also a half wave rectified sine wave of corresponding amplitude. For a 60 Hz line frequency about 1666 samples of digital sine wave (waveform 5) generate 2 of the half-wave rectified sine waves. Phase shifting the switching of the MOSFETs in the full-bridge legs with varying phase results in the Zero Voltage Switching lowering the conduction

losses. At the same PSFB operating in ZVS mode also allows higher frequency switching thereby reducing the switching losses.

In an example, the present invention provides an inverter device. The device includes a slave inverter circuit configured to generate a rectified DC waveform and an active ripple cancellation boost circuit coupled to the slave inverter circuit and being configured coupled to a DC source from a plurality of solar cells and configured to filter an AC current ripple back to the DC source and boost the DC voltage to an intermediary 12-15 voltage range. The device also has a wave shaper circuit coupled to the slave inverter circuit and comprising a phase shift zero voltage switching full bridge circuit and a rectifier energy recovery circuit. The phase shift zero voltage switching full bridge circuit is configured to shape the DC source to a half wave rectified 120V to 240V waveform. The rectifier energy recovery circuit is configured to recovery energy during a switching operation to cause formation of the waveform. The device also includes an analog mixed signal or digital controller module configured to generate a PWM waveform and synchronize the rectified waveform to a grid voltage and configured to manage a plurality of sense circuits coupled to a plurality of solar cells to record a cell group voltage and cell group current.

In a specific embodiment, the inverter device has variations. The inverter device further comprising a master control module configured to a plurality of analog mixed signal or digital controller modules. The master control module is configured to generate a reference signal for each of the analog mixed signal control modules and turn off/on the rectified waveform from each of the inverter devices to a power-line grid. The master controller module comprising a detector device coupled to the power-line grid to measure a grid voltage and a grid frequency at any given time. The master control module is configured to turn on/off each of the inverter devices using information from the grid voltage and/or the grid frequency. The master controller module is configured on a solar module by attachment to a backplane of the solar module. The backplane being is substantially free from a junction box or power aggregator. The inverter device further comprises a plurality of solar cell groups, each of the solar cell groups having a DC input to the DC slave circuit. The master controller is configured to control an unfold circuit, which comprise an H-bridge circuit with one of an SCR, MOSFET, or an IGBT circuit. The un-folder circuit is controlled with a closed loop control algorithm for delivery of power to a power-line grid by aggregating a plurality of current waveforms generated by a plurality of slave inverter circuits.

In an alternative example, the master controller and the analog mixed signal or digital controllers are configured to communicate to exchange a plurality of reference signals and at least one voltage/current level from of each of the solar cell groups. The master controller generates a reference voltage waveform proportional to a power line grid voltage within a determined desired limit at the power line grid frequency. The master controller generates an instant shutoff signal which when received by the analog mixed signal or digital controller power down a plurality of switching circuits of the slave inverter circuit within 500 milliseconds of an initiation of the generation of the instant shutoff signal. The master controller generates an additional sine-wave modulated onto an output voltage waveform to distort a power-line grid voltage waveform which in a presence of a power line grid is free from any alteration of the power line grid voltage waveform or the additional sine wave modulated onto the output voltage wave-

form distorts the output voltage waveform in absence of the power line grid to initiate the shut off of the slave inverter circuit.

In an example, the slave inverter circuit controlled by an analog mixed signal or digital controller continuously monitors a power output from a cell group coupled to the slave inverter circuit to maximize the power output by varying a power level and tracking a maximum power point (MPPT) of the cell group. The slave inverter circuit controlled by an analog mixed signal or digital controller maximizes the power output to a varying power level caused by a change in irradiation provided on the cell group. The slave inverter circuit controller by an analog mixed signal or digital controller comprises phase lock loop (PLL) circuit to synchronize a reference voltage sampled by a master circuit to shape an output current and a voltage waveform. The slave circuit comprises a power loss reduction circuit configured to reduce an energy loss in a diode bridge generating the half-wave rectified waveform, the energy loss circuit being provided by a CMOS circuit or SiC circuit.

In an example, the back plane comprises a plurality of DC inputs from the solar cell groups fed into a printed circuit board of the back plane at a plurality of pre-defined points to couple the plurality of pre-defined points with the plurality of slave inverter circuits and an auxiliary power supply. The auxiliary power supply provides power to operate the plurality of slave inverter circuits, the master controller module, the un-folder circuit, a communication controller and other associated circuits. The auxiliary power supply adapted to be triggered at a plurality of voltage levels associated with a design of the group of cells. The wave shaper circuit comprising a Phase shift full bridge zero voltage switch (ZVS) circuit and a diode loss recovery circuit.

In an example, the present invention also includes related methods to carryout the functionality of the circuits and systems described herein. In an example, the present invention provides a method for operating an inverter device. The method includes generating a rectified DC waveform using a slave inverter circuit, filtering an AC current ripple back to the DC source, boosting the rectified DC waveform to an intermediary 12-15 voltage range, shaping the rectified DC waveform to a half wave rectified 120V to 240V waveform, recovering energy using the rectifier energy recovery circuit during a switching operation, generating a PWM waveform using either an analog mixed signal module or digital controller module, synchronizing the rectified DC waveform to a grid voltage, and managing a plurality of sense circuits coupled to the plurality of solar cells to record a cell group voltage and a cell group current. In an example, the present method further includes generating a reference signal for each of the analog mixed signal control modules to turn off/on the rectified DC waveform from each of the inverter devices to a power-line grid. It should be understood that the description recited above is an example of the disclosure and that modifications and changes to the examples may be undertaken which are within the scope of the claimed disclosure. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements, including a full scope of equivalents.

What is claimed is:

1. An inverter device comprising:

a plurality of slave inverter circuits each configured to generate a rectified DC waveform, each slave inverter circuit comprising:

an active ripple cancellation boost circuit coupled to a DC source from a plurality of solar cells and config-

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ured to filter an AC current ripple back to the DC source and boost a DC voltage to an intermediary 12-15 voltage range;

a wave shaper circuit comprising a phase shift zero voltage switching full bridge circuit and a rectifier energy recovery circuit, the phase shift zero voltage switching full bridge circuit configured to shape the rectified DC waveform to a half wave rectified 120V to 240V waveform ("half wave rectified waveform"), the rectifier energy recovery circuit being configured to recover energy during a switching operation in formation of the rectified DC waveform;

an analog mixed signal module or digital controller module configured to generate a PWM waveform and synchronize the rectified DC waveform to a grid voltage and configured to manage a plurality of sense circuits coupled to the plurality of solar cells to record a cell group voltage and a cell group current; and

a master control module coupled to the plurality of slave inverter circuits, the master control module comprising a detector device configured to be coupled to a power grid to measure a grid voltage and a grid frequency, the master control module being configured to turn on or off the inverter device using information from the grid voltage or the grid frequency.

2. The inverter device of claim 1, wherein the master control module is configured to generate a reference signal for each of the analog mixed signal control modules or each of the plurality of digital controller modules and turn off or on the rectified DC waveform from each of the slave inverter circuits to the power grid.

3. The inverter device of claim 1 wherein the master controller module is attached to a backplane of a solar module, the backplane being substantially free from a junction box or power aggregator.

4. The inverter device of claim 3, wherein the solar module comprises a plurality of solar cell groups including the plurality of solar cells, each of the solar cell groups having a DC input to one of the slave inverter circuits.

5. The inverter device of claim 1 wherein the master controller is configured to control an unfold circuit, the unfolded circuit comprising of an H-bridge circuit with one of an SCR, MOSFET, or an IGBT circuit.

6. The inverter device of claim 5 wherein the unfold circuit is controlled with a closed loop control algorithm for delivery of power to the power grid by aggregating a plurality of current waveforms generated by the plurality of slave inverter circuits.

7. The inverter device of claim 4 wherein the master controller and the analog mixed signal or digital controllers are configured to communicate to exchange a plurality of reference signals and at least one voltage or current level from of each of the solar cell groups.

8. The inverter device of claim 1 wherein the master controller is configured to generate a reference voltage waveform proportional to a power grid voltage within a determined desired limit at the power grid frequency.

9. The inverter device of claim 1 wherein the master controller is configured to generate an instant shutoff signal which when received by the analog mixed signal or digital controller power down a plurality of switching circuits of the slave inverter circuit within 500 milliseconds of an initiation of the generation of the instant shutoff signal.

10. The inverter device of claim 9 wherein the master controller generates an additional sine-wave modulated onto

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an output voltage waveform to distort a power grid voltage waveform which in a presence of a power grid is free from any alteration of the power grid voltage waveform or the additional sine wave modulated onto the output voltage waveform distorts the output voltage waveform in absence of the power grid to initiate the shut off of the slave inverter circuit.

11. The inverter device of claim 4 wherein the analog mixed signal or digital controller continuously monitors a power output from the solar cell group coupled to the slave inverter circuit to maximize the power output by varying a power level and tracking a maximum power point (MPPT) of the solar cell group.

12. The inverter device of claim 11 wherein the analog mixed signal or digital controller maximizes the power output to a varying power level caused by a change in irradiation provided on the solar cell group.

13. The inverter device of claim 1 wherein the analog mixed signal or digital controller comprises a phase lock loop (PLL) circuit to synchronize a reference voltage sampled by a master circuit to shape an output current and a voltage waveform.

14. The inverter device of claim 1 wherein each slave inverter circuit comprises a power loss reduction circuit configured to reduce an energy loss in a diode bridge generating the half-wave rectified waveform, the energy loss circuit being provided by a CMOS circuit or SiC circuit.

15. The inverter device of claim 4 wherein the plurality of slave inverter circuits are attached to the back plane of the solar module, the back plane comprising a plurality of DC inputs from the solar cell groups fed into a printed circuit board of the back plane at a plurality of pre-defined points to couple the plurality of pre-defined points with the plurality of slave inverter circuits and an auxiliary power supply, the auxiliary power supply providing power to operate the plurality of slave inverter circuits and the master controller module.

16. The inverter device of claim 15 wherein the auxiliary power supply is adapted to be triggered at a plurality of voltage levels associated with a design of the group of cells.

17. A method for operating an inverter device, the method comprising:

generating a rectified DC waveform using a slave inverter circuit;

filtering an AC current ripple back to the DC source;

boosting the rectified DC waveform to an intermediary 12-15 voltage range;

shaping the rectified DC waveform to a half wave rectified 120V to 240V waveform;

recovering energy using the rectifier energy recovery circuit during a switching operation;

generating a PWM waveform using either an analog mixed signal module or digital controller module;

synchronizing the rectified DC waveform to a grid voltage;

managing a plurality of sense circuits coupled to the plurality of solar cells to record a cell group voltage and a cell group current;

measuring the grid voltage and a grid frequency with a detector device; and

selectively turning on or off the inverter device based on the measured grid voltage or the grid frequency.

18. The method of claim 17 further comprising generating a reference signal for each of the analog mixed signal control modules to turn off or on the rectified DC waveform from each of the inverter devices to a power grid.

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